CLAIMS

In the Claims

1. A method of performing block decoding on a received block of symbols previously coded column-wise with an (N, K) linear block code and row-wise with an error detection code, comprising:

identifying a codeword corresponding to a column of the received block where an undetected symbol error is located;

determining a location of the undetected symbol error in the codeword;

marking a row of the received block containing the undetected symbol error as an erased row; and

performing block decoding for the received block with the marked erased row.

2. The method of claim 1, further comprising:

deriving an estimate of an un-erased systematic row of the received block;

comparing the un-erased systematic row against its estimate; and

identifying a location of an unmatched symbol between the un-erased systematic row and its estimate, and wherein the codeword is identified as corresponding to the column containing the unmatched symbol.

3. The method of claim 2, wherein the estimate of the un-erased systematic row is derived by

marking the un-erased systematic row as an erased row;

forming a reduced received block comprised of K un-erased rows of the received block; and

multiplying an inverse generator matrix for the K un-erased rows with the reduced received block.

4. The method of claim 1, wherein the location of the undetected symbol error in the codeword is determined by performing error location on the codeword based on a particular block decoding scheme.

5. The method of claim 1, wherein the performing block decoding includes

forming a reduced received block comprised of K un-erased rows of the received block;

forming a reduced generator matrix comprised of K rows of a generator matrix corresponding to the K un-erased rows;

inverting the reduced generator matrix; and

multiplying the inverted generator matrix with the reduced received block.

6. The method of claim 1, further comprising:

marking each row of the received block as either an erased row or an un-erased row until at least (K+1) un-erased rows are found.

7. The method of claim 6, wherein each row is marked as an erased row or an un-erased row based on a result of a cyclic redundancy check (CRC) test.

8. The method of claim 1, further comprising:

determining the number of erased rows in the received block.

9. The method of claim 8, further comprising:

performing erasure-only correction block decoding if the number of erased rows is equal to (D-2) or (D-1).

10. The method of claim 8, further comprising:

performing erasure-and-error correction block decoding if the number of erased rows is less than or equal to (D-3).

11. The method of claim 10, further comprising:

determining the number of erased systematic rows in the received block; and

performing erasure-and-error correction block decoding if the number of erased systematic rows is less than or equal to (K-1).

12. The method of claim 8, further comprising:

declaring an error if the number of erased rows exceeds (D-1).

13. The method of claim 1, wherein the (N, K) linear block code is a Reed-Solomon code.

14. A method of performing block decoding on a received block of symbols previously coded column-wise with an (N, K) linear block code and row-wise with an error detection code, comprising:

marking each row of the received block as either an erased or an un-erased row until at least (K+1) un-erased rows are found;

deriving an estimate of an un-erased systematic row of the received block;

comparing the un-erased systematic row against its estimate;

identifying an unmatched symbol between the un-erased systematic row and its estimate;

identifying a codeword corresponding to a column of the received block containing the unmatched symbol;

determining a location of a symbol error in the codeword based on a particular block decoding scheme;

marking a row of the received block containing the symbol error as an erased row; and

performing block decoding for the received block with the marked erased row.

15. A computer program product for performing block decoding on a received block of symbols previously coded column-wise with an (N, K) linear block code and row-wise with an error detection code, comprising:

code for identifying a codeword corresponding to a column of the received block where an undetected symbol error is located;

code for determining a location of the undetected symbol error in the codeword;

code for marking a row of the received block containing the undetected symbol error as an erased row;

code for performing block decoding for the received block with the marked erased row; and

a computer-usable medium for storing the codes.

16. The computer program product of claim 15, further comprising:

code for deriving an estimate of an un-erased systematic row of the received block;

code for comparing the un-erased systematic row against its estimate; and

code for identifying a location of an unmatched symbol between the un-erased systematic row and its estimate, and wherein the codeword with the undetected symbol error is identified as corresponding to the column containing the unmatched symbol.

17. The computer program product of claim 16, wherein the code for deriving the estimate of the un-erased systematic row includes:

code for marking the un-erased systematic row as an erased row;

code for forming a reduced received block comprised of K un-erased rows of the received block; and

code for multiplying an inverse generator matrix for the K un-erased rows with the reduced received block.

18. The computer program product of claim 15, wherein the code for performing block decoding includes:

code for forming a reduced received block comprised of K un-erased rows of the received block;

code for forming a reduced generator matrix comprised of K rows of a generator matrix corresponding to the K un-erased rows;

code for inverting the reduced generator matrix; and

code for multiplying the inverted generator matrix with the reduced received block.

19. A memory communicatively coupled to a digital signal processing device (DSPD) capable of interpreting digital information to:

identify a codeword corresponding to a column of the received block where an undetected symbol error is located;

determine a location of the undetected symbol error in the codeword;

mark a row of the received block containing the undetected symbol error as an erased row; and

perform block decoding for the received block with the marked erased row.

20. A digital signal processor comprising comprising: a first unit operative to receive a block of symbols previously coded column-wise with an (N, K) linear block code and row-wise with an error detection code and to mark each row of the received block as either an erased row or an un-erased row until at least (K+1) un-erased rows are found; and

a second unit operative to identify a codeword corresponding to a column of the received block where an undetected symbol error is located, determine the location of the undetected symbol error in the codeword, mark a row of the received block containing the undetected symbol error as an erased row, and perform block decoding for the received block with the marked erased row.

21. The digital signal processor of claim 20, wherein the second unit is further operative to derive an estimate of an un-erased systematic row of the received block, compare the un-erased systematic row against its estimate, and identify a location of an unmatched symbol between the un-erased systematic row and its estimate, and wherein the codeword with the undetected symbol error is identified as corresponding to the column containing the unmatched symbol.

22. The digital signal processor of claim 20, wherein the second unit is further operative to mark the un-erased systematic row as an erased row, form a reduced received block comprised of K un-erased rows of the received block, and multiply an inverse generator matrix for the K un-erased rows with the reduced received block.

23. The digital signal processor of claim 20, wherein the second unit is further operative to form a reduced received block comprised of K un-erased rows of the received block, form a reduced generator matrix comprised of K rows of a generator matrix corresponding to the K un-erased rows, invert the reduced generator matrix, and multiply the inverted generator matrix with the reduced received block.

24. A decoder comprising:

a first decoder operative to receive a block of symbols previously coded column-wise with an (N, K) linear block code and row-wise with an error detection code and to mark each row of the received block as either an erased row or an un-erased row until at least (K+1) un-erased rows are found; and

a second decoder operative to identify a codeword corresponding to a column of the received block where an undetected symbol error is located, determine the location of the undetected symbol error in the codeword, mark a row of the received block containing the undetected symbol error as an erased row, and perform block decoding for the received block with the marked erased row.

25. The decoder of claim 24, wherein the first decoder is operative to mark each row as an erased row or an un-erased row based on a result of a cyclic redundancy check (CRC) test.

26. The decoder of claim 24, wherein the (N, K) linear block code is a Reed-Solomon code.

27. A decoding apparatus comprising:

means for marking each row of a received block, previously coded column-wise with an (N, K) linear block code and row-wise with an error detection code, as either an erased row or an un-erased row until at least (K+1) un-erased rows are found;

means for identifying a codeword corresponding to a column of the received block where an undetected symbol error is located;

means for determining a location of the undetected symbol error in the codeword;

means for marking a row of the received block containing the undetected symbol error as an erased row; and

means for performing block decoding for the received block with the marked erased row.

28. The decoding apparatus of claim 27, further comprising:

means for deriving an estimate of an un-erased systematic row of the received block;

means for comparing the un-erased systematic row against its estimate; and

means for identifying a location of an unmatched symbol between the un-erased systematic row and its estimate, and wherein the codeword with the undetected symbol error is identified as corresponding to the column containing the unmatched symbol.

29. The decoding apparatus of claim 28, wherein the means for performing block decoding includes:

means for marking the un-erased systematic row as an erased row;

means for forming a reduced received block comprised of K un-erased rows of the received block; and

means for multiplying an inverse generator matrix for the K un-erased rows with the reduced received block

30. The decoding apparatus of claim 27, wherein the means for performing block decoding includes:

means for forming a reduced received block comprised of K un-erased rows of the received block;

means for forming a reduced generator matrix comprised of K rows of a generator matrix corresponding to the K un-erased rows;

means for inverting the reduced generator matrix; and

means for multiplying the inverted generator matrix with the reduced received block.

31. A receiver unit in a wireless communication system, comprising:

a receiver operative to process a received signal to provide data samples;

a demodulator operative to process the data samples to provide a received block of symbols;

a first decoder operative to mark each row of the received block as either an erased row or an un-erased row; and

a second decoder operative to identify a codeword corresponding to a column of the received block where an undetected symbol error is located, determine the location of the undetected symbol error in the codeword, mark a row of the received block containing the undetected symbol error as an erased row, and perform block decoding for the received block with the marked erased row.

32. The receiver unit of claim 31, further comprising:

a third decoder operative to receive and decode demodulated data from the demodulator in accordance with a particular convolutional decoding scheme to provide the received block of symbols.